REMARKS

Claim Rejections Under 35 USC §103(a)

Claims 25-39 and 47-53 have been rejected under 35 USC §103(a) as being unpatentable over Hembree et al. (US Patent No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227), Pedder (US Patent No. 5,717,245) and Gilmour et al. (US Patent No. 5,391,917).

The rejections under 35 USC §103 are traversed for the reasons to follow. In the alternative, the rejections under 35 USC §103 are submitted to have been overcome by the amendments to the claims.

Summary of the Invention

Claims 25-39 and 47-53 are directed to a "semiconductor component". The component includes a substrate 10 (Figure 2) and a conductive layer 14 (Figure 2) substantially covering a surface of the substrate 10. In addition, the component includes conductors 16 (Figure 2) on the substrate 10, and a semiconductor die 20 (Figure 2E, 3A or 7) in electrical communication with the conductors 16.

Each conductor 16 is defined by a pair of grooves 15 (Figure 2) which comprise ablated portions of the conductive layer 14. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 14 separated by the grooves 15, and by remaining portions of the conductive layer 14 having edges defined by the grooves 15. As shown in Figure 2, each conductor 16 can include a bond pad 18 (pads or contacts in the claims) configured for flip chip mounting or wire bonding the die 20. Each conductor 16 can also include a contact pad 22 (contacts in the claims) configured for electrical connection to outside circuitry. In the case of wire bonding, an opening 40 (Figure 3A) can be laser machined in the conductive layer 14 for attaching the die 20 to the substrate. As shown in Figure 5A, the substrate 10BGA can also include conductive

vias 58 in electrical communication with the conductors 16BGA, and contact balls 66 in electrical communication with the conductive vias 58.

35 USC §103 Rejections over Hembree et al. in view of Frankeny et al., Pedder and Gilmour et al.

Independent claims 25, 30, 35, 47 and 52 have been amended to remove the recitation of the conductors being defined by "laser machined grooves". In place of this recitation, the independent claims have been amended to emphasize the structure of the semiconductor component which results from the laser machining fabrication process.

Specifically, independent claim 25 states that the grooves comprise "ablated portions of the conductive layer". Antecedent basis for this recitation is provided on page 3, lines 16-18, and on page 8, lines 22-24 of the specification. Independent claim 25 also states that the conductors comprise "portions of the conductive layer electrically isolated by the grooves and separated by remaining portions of the conductive layer having edges defined by the grooves". Antecedent basis for this recitation is provided on page 8, lines 8-21 of the specification. In addition, the recited features are shown in Figures 2–2D of the drawings.

Independent claim 30 is similar to independent claim 25, and states that the conductive layer comprises "a metal foil attached to and substantially covering the surface". Antecedent basis for this recitation is provided on page 7, lines 22-23 of the specification.

Independent claim 35 is similar to independent claim 25, and states that the conductors comprise "portions of the conductive layer separated by remaining portions of the conductive layer, the conductors defined and electrically isolated by a plurality of grooves comprising ablated portions of the conductive layer, each conductor and each remaining portion defined by at least one pair of grooves".

Antecedent basis for this recitation is provided on page 8, lines 8-21 of the specification.

Independent claim 47 is similar to independent claim 25, and states that the conductors comprise "first contacts on first ends thereof and second contacts on second ends thereof" (e.g., bond pads 18 and contact pads 22 in Figure 2C).

Independent claim 52 is similar to independent claim 25, and recites "a plurality of conductive vias through the substrate in electrical communication with the conductors" (e.g., conductive vias 58 in Figure 5A).

The primary reference to Hembree et al. discloses a temporary semiconductor package for testing semiconductor dice. The package 10 (Figure 1) includes an interconnect 16 having raised contact members 60 (Figure 4) for making electrical connections with bond pads 62 on the die 12 (column 6, lines 27-30). In addition, the interconnect 16 includes conductive layers 68 (Figure 5) on the contact members 60, and conductive traces 58 (Figure 4) in electrical communication with the conductive layers 68 (column 6, lines 37-40).

Although the conductive traces 58 in Hembree et al. can be formed of a conductive layer, and perform the same function as the presently claimed conductors (i.e., signal transmission), the conductive traces 58 are not defined by grooves which comprise "ablated portions of a conductive layer". In addition, there are no "remaining portions" of a conductive layer which separate adjacent conductive traces 58, and which have edges defined by the grooves. Rather, if a conventional subtractive process, such as etching through a mask, is used to form the conductive traces 58 in Hembree et al., then there would be no grooves, and no remaining portions of an initially deposited conductive layer, because all of the material except the conductive traces 58 would have been etched away. The presently claimed conductors are an improvement

over conventional conductors, because they can be made extremely small, closely spaced and with precise dimensional tolerances using laser machining.

Frankeny et al. also does not disclose or suggest conductors defined by grooves which comprise "ablated portions of a conductive layer", and "remaining portions" of a conductive layer which separate adjacent conductors. Rather, Frankeny et al. teaches "a laser drilling operation" at column 5, line 65 to form a conductive via. However, the copper layer (i.e., conductors) in Figure 5 of Frankeny et al. is formed using "traditional plating, photoimaging, and etching techniques common to printed wiring board manufacture."

Pedder also does not disclose or suggest conductors defined by grooves which comprise "ablated portions of a conductive layer", and "remaining portions" of a conductive layer which separate adjacent conductors. Pedder discloses a BGA device having a multilayered substrate 12 that includes microstrip trimming stubs 94, 95 which are trimmed using a laser (column 8, lines 46-54). However, the trimming stubs 94, 95 are formed using a conventional metallization process (column 4, lines 11-18), and are then trimmed to a desired length using a laser to achieve electrical tuning (column 6, lines 60-63). Although the length of the trimming stubs 94, 95 is adjusted by laser trimming, the trimming stubs 94, 95 are not defined by grooves which comprise ablated portions of a conductive layer. Rather, the grooves which define the trimming stubs 94, 95 are already present, and the laser merely removes a portion of the stubs 94, 95.

Gilmour et al. also does not disclose or suggest conductors defined by grooves which comprise "ablated portions of a conductive layer", and "remaining portions" of a conductive layer which separate adjacent conductors. Gilmour et al. teaches laser machined vias having a spacing of 40 μm. In contrast, with the present invention the laser

machined grooves can be as small as about 5 μm, such that the conductors also have a spacing of only about 5 μm.

As the cited combination of references "taken as a whole" does not teach or suggest the primary features of the present semiconductor device, the amended independent claims are submitted to be unobvious over the combination of references.

Applicant would further argue that one skilled in the art at the time of the invention would have no incentive to combine the references in the manner of the Office Action. In this regard, the Office Action states the incentive as: "so that the resonance characteristics, electrical performance and reliability of the contacts/device can be improved using Pedder, Gilmour et al. and Frankeny et al's conductor structure in Hembree's component".

Applicant would argue that the Hembree et al. temporary semiconductor package is already reliable, and it is unclear how any of the secondary references would make the package more reliable. For example, the conductive traces 58 in Hembree et al. have no need for improved resonance characteristics because they do not function in the same manner as the resonator 60 (Figure 5) in Pedder, which is a passive circuit element such as a filter. Further, it is unclear how using laser trimming of conductive stubs as taught by Pedder, laser drilling of vias as taught by Frankeny, or laser machined vias as taught by Gilmour et al. could all be incorporated into the Hembree et al. temporary package.

Applicant would further argue that the combination of references results from a reading of the present disclosure, and the need to substantiate a 35 USC §103 rejection, rather than from the teachings of the prior art existing at the time of the present invention.

Conclusion

In view of the above amendments and arguments, favorable consideration and allowance of claims 25-39 and 47-53 is requested. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

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Date of Signature

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Marked Version Of Claims Showing Changes

25. (five times amended) A semiconductor component comprising:

a substrate having a [first] surface;

[and an opposing second surface;]

a [blanket deposited] conductive layer [on] substantially covering the [first] surface;

a plurality of conductors on the [first] surface defined by a plurality of [laser machined] grooves comprising ablated portions of [through] the conductive layer [to the substrate], the conductors comprising portions of the conductive layer electrically isolated by the grooves and separated by remaining portions of the conductive layer having edges defined by the grooves; and

at least one semiconductor die on the substrate in electrical communication with the conductors.

[;]

[a plurality of conductive vias in the substrate from the first surface to the second surface in electrical communication with the conductors; and]

[a plurality of external contacts on the second surface in electrical communication with the conductive vias.]

30. (five times amended) A semiconductor component comprising:

a substrate having a surface;

a [blanket deposited] conductive layer comprising a metal foil attached to and substantially covering the surface;

[and having a thickness;]

a plurality of conductors [and pads] on the surface defined by a plurality of [laser machined] grooves comprising ablated portions of the metal foil, [through the

thickness of the conductive layer to the substrate extending on the surface in a plurality of directions,] each conductor [and each pad] comprising a portion of the [conductive layer] metal foil electrically isolated by at least one pair of [laser machined] grooves and separated from an adjacent conductor by a remaining portion of the metal foil; and

a semiconductor die flip chip mounted or wire bonded to the substrate in electrical communication with the conductors.

[pads.]

35. (five times amended) A semiconductor component comprising:

a substrate having a surface;

a [blanket deposited] conductive layer [on] substantially covering the surface;

a plurality of conductors on the surface comprising portions of the conductive layer separated by remaining portions of the conductive layer, the conductors defined and electrically isolated by a plurality of [laser machined] grooves [through] comprising ablated portions of the conductive layer, [to the substrate,] each conductor and each remaining portion defined by at least one pair of [laser machined] grooves;

a semiconductor die on the substrate in electrical communication with the conductors.

[; and]

[an encapsulant on the substrate covering the die and the conductive layer.]

47. (five times amended) A semiconductor component comprising:

a substrate having a surface;

a [blanket deposited] conductive layer substantially covering the surface; and

a plurality of conductors on the surface defined by a plurality of [laser machined] grooves [through] comprising ablated portions of the conductive layer, [to the surface and extending in a plurality of directions on the surface,] the conductors comprising portions of the conductive layer which are electrically isolated from one another by the [laser machined] grooves and separated by remaining portions of the substrate having edges defined by the grooves, the conductors comprising [portions of the conductive layer including] first contacts on first ends thereof [configured for bonding,] and second contacts on second ends thereof [configured for electrical connection to external circuitry]; and

a semiconductor die on the substrate bonded to the first contacts.

52. (four times amended) A semiconductor component comprising:

a substrate having a surface;

a [blanket deposited] conductive layer [on] substantially covering the surface;

a plurality of conductors on the surface defined by a plurality of [first laser machined] grooves [through] comprising ablated portions of the conductive layer, [to the surface,] the conductors comprising portions of the conductive layer electrically isolated by the grooves and separated by remaining portions of the conductive layer having edges defined by the grooves;

[a plurality of contacts on the conductors defined by a plurality of second laser machined grooves through the conductive layer to the surface;]

a plurality of conductive vias through the substrate in electrical communication with the conductors; and

a semiconductor die on the substrate in electrical communication with the conductors.

[contacts.]